UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,162	11/17/2003	Shiro Dosho	60188-706	9457

7590 06/02/2005

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
NGUYEN, MINH T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,162	DOSHO ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 6-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 6* is/are allowed.

6)☒ Claim(s) *2,3 and 7* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 4/7/05 has been received and entered in the case. The amendment and argument presented therein overcome the informality objections, indefiniteness rejections and prior art rejections noted in the previous Office action, therefore, these are withdrawn. New grounds of rejections necessitated by the amendment are needed as set forth below. This action is FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,488,317, issued to Webster et al. in view of US Patent No. 6,060,922, issued to Chow et al.

As per claim 2, Webster discloses a 50 percent duty cycle production circuit (figure 3, Webster calls the circuit is an output driver, column 4, lines 27. However, the circuit is also functioned as a 50 percent duty cycle production circuit because the circuit has the same structure as the claimed circuit as discussed herein below) comprising:

a delay unit (transistors 34 and 36) for receiving a first clock signal (at the I/O node) in which a first logic value has a shorter period of time per cycle than a second logic value (the structural of the claimed delay unit is not distinguishable from the structural of the Webster's delay unit based on this recited limitation, MPEP 2114. It is clear that the Webster's delay unit is able to receive a clock signal with the recited characteristics), delaying the first clock signal, and outputting a second clock signal which transitions to the second logic value at a timing at which the period of time equivalent to a half cycle has elapsed since the first clock signal transitioned to the first logic value (this limitation is met because the Webster's delay unit is configured to function as a resistor just like the delay unit shown in Fig. 1 of the present invention, see column 4, lines 49-54, i.e., transistors 34 and 36 are ON and compare with the delay unit shown in Fig. 1 of the present invention, i.e., transistors 111 and 112 are configured to be ON); and

a clock-signal output unit (transistors 38 and 40) for outputting a third clock signal (Y) based on the first and second clock signals,

wherein the clock-signal output unit comprises: a first output unit (transistor 39) for setting the third clock signal (Y) at a first logic output value with either one of the first logic value and the second logic value in response to the transition of the first clock signal to the first logic value (for example, a HIGH of the first clock signal at the gate of transistor 38 provides a LOW at node Y); and a second output unit (transistor 40) for setting the third clock signal (Y) at a second logic output value with the other of the first logic value and the second logic value in response to the transition of the second clock signal (at the gate of transistor 40) to the second logic value (for example, a LOW of the second clock signal at the gate of transistor 40 provides a HIGH at node Y).

Webster does not explicitly disclose that a frequency divider circuit is connected to the I/O input terminal for producing the first clock signal as called for in the claim.

Chow discloses a duty cycle control circuit (figure 3) which has first and second output units (transistors P1 and N1) wherein the output units are functioned as an output driver circuit. He further explicitly discloses a frequency divider circuit (the FINITE STATE MACHINE, column 3, lines 53-57) for dividing an input clock signal (I/P CLOCK having frequency F) to generate the first clock signal having frequency F/N before providing the first clock signal to the output driver circuit. Further, he explicitly discloses the advantage of adding a frequency divider circuit is to reduce the power consumption of the entire circuit because of the lower operating frequency (column 2, lines 25-28).

It would have been obvious to one skilled in the art at the time of the invention was made to include a frequency divider circuit as taught by Chow in the Webster's duty cycle clock signal producing circuit to reduce the first frequency clock signal in the Webster's duty cycle clock signal producing circuit. The motivation and/or suggestion would be to reduce the power consumption of the Webster's duty cycle clock signal producing circuit by lower the operating frequency when the Webster's circuit is used in applications which do not require a high operating frequency.

As per claim 3, Webster further discloses:

the first output unit includes a first transistor which is of either one of n-channel type and p-channel type and whose gate receives the first clock signal (as shown, transistor 38 is N type),

the second output unit includes a second transistor which is of the other of n-channel type and p-channel type, whose gate receives the second clock signal and whose drain is connected to

a drain of the first transistor (as shown, transistor 40 is the other type, i.e., P type, the drain is connected as recited), and

the third clock signal is based on a signal output from the common drain of the first and second transistors (at node Y).

As per claim 7, Webster further discloses:

the delay unit includes a transistor (NMOS 36) whose gate is supplied with a predetermined voltage (VCC, column 4, line 50) and of which either one of a source and a drain receives the first clock signal to output the second clock signal from the other of the drain and the source (as shown in Fig. 3), and

the predetermined voltage supplied to the gate of the transistor is above a gate threshold value in the case where the transistor is an n-channel transistor while the predetermined voltage supplied to the gate of the transistor is below the gate threshold value in the case where the transistor is a p-channel transistor (this is the condition for an NMOS transistor ON, note: transistor NMOS 36 is ON, column 4, lines 50-51).

Response to Arguments

3. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

4. Claims 1 and 6 are allowed for the reason noted in the previous Office action.

5. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 8 is allowable because the prior art of record fails to disclose or suggest the inclusion of the limitation that from the input terminal of the duty-cycle clock signal production circuit, the numbers of the n-channel and p-channel transistors in which a signal travels in the rising or falling of the third clock signal are the same. The inclusion of the recited limitation defines patentability over the prior art of record because it defines a distinctive structure of the frequency divider in combination with the output unit which is not taught by the prior art of record, alone or in combination.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/26/05

Minh Nguyen
Primary Examiner
Art Unit 2816